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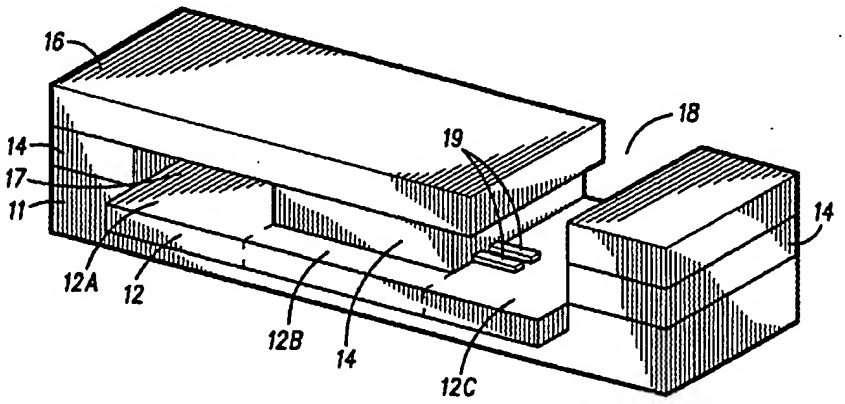
(54) Title: SEMICONDUCTOR WAFER LEVEL PACKAGE

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(57) Abstract: A semiconductor wafer level package used to encapsulate a device fabricated on a semiconductor substrate wafer (11) before dicing of the wafer into individual chips. A cap wafer (16) may be bonded to the semiconductor subtrate using a low temperature frit glass layer (14) as a bonding agent. The frit glass layer (14) is in direct contact with the device. A hermetic seal is formed by a combination of the semiconductor substrate wafer (11), the cap wafer (16) and the first glass layer (14). A second embodiment of the package (21) does not contain a cap wafer.

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# SEMICONDUCTOR WAFER LEVEL PACKAGE

## FIELD OF THE INVENTION

This present invention relates to the wafer-scale packaging of monolithically integrated sensors and actuators and of integrated circuits in general.

## BACKGROUND OF THE INVENTION

The advancement and miniaturization of integrated circuit technologies through the application of micromachining processes derived from standard microelectronic fabrication technologies has required the introduction of new packaging techniques to protect various elements of the sensor system from unwanted exposure during manufacturing or in the system application. Ideally, these techniques would be applied at the wafer scale, prior to die singulation, as has been described in U.S. Patent #5,323,051. Wafer scale packaging provides significant enhancements for manufacturing and has resulted in the introduction of many micromachined sensor components more difficult or impossible to produce with other techniques.

The performance enhancement gained through the monolithic integration of control circuitry along with micromachined sensing elements again taxes the potential of wafer scale packaging techniques. Wafer scale packaging

using a glass frit as the bonding medium requires temperatures not typically compatible with standard microelectronics processing for the bond process, and often involves frit materials containing elemental components deleterious to active circuitry. Even with the resolution of such limitations, neither performance nor area utilization is enhanced significantly if the wafer scale packaging requires unique bond areas.

Accordingly, there exists a need for a wafer level package in which glass frit may be formed in contact with active components of a semiconductor device. Further, such a semiconductor package, that may or may not contain a cap wafer, provides a reliable device without compromising the characteristics of the components.

## SUMMARY OF THE INVENTION

This present invention provides a semiconductor wafer-level package in which glass frit is formed directly in contact with the devices or active circuitry in the monolithic device. This could be embodied using wafer bond or by direct application of glass frit to the devices. This package may be used to encapsulate a monolithically-integrated sensor structure, to protect an integrated circuit from unwanted exposure to environmental or electromagnetic interactions, or to create wafer-scale protected integrated circuits and systems for flip-chip packaging applications. A preferred embodiment includes a cap wafer bonded to the semiconductor substrate,

which may include integrated circuits and sensors. This bond is formed using a pattern of frit glass as a pattern such that any sealed volumes formed by the cap wafer, frit glass, and semiconductor substrate are hermetically sealed. Integrated circuits (devices), can exist beneath the frit glass seal. Another preferred embodiment includes direct application of a pattern of glass frit to a semiconductor substrate such that regions of the substrate are hermetically sealed. Integrated circuits (devices) can exist directly beneath the frit glass.

## BRIEF DESCRIPTION OF THE DRAWING

The present invention will be better understood from a reading of the following detailed description, taken in conjunction with the accompanying drawing figures in which:

Figure 1 shows a perspective cross-sectional view of a device encapsulated within a semiconductor wafer level package containing a cap wafer in accordance with a first preferred embodiment of the present invention.

Figure 2 illustrates a perspective cross-sectional view of an encapsulated device excluding a cap wafer in accordance with a second preferred embodiment of the invention.

For simplicity and clarity of illustration, the figures illustrate the general invention, and descriptions and details of well-known features and techniques are omitted to avoid excessive complexity. The figures are not necessarily drawn to scale, and the same reference numerals in different figures denote the same elements. It is further understood that the embodiments of the invention described herein are capable of being manufactured or operated in other orientations than described or illustrated herein.

## DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Figure 1 shows a cross sectional view of a device 12, which is encapsulated in a wafer scale package 21 in accordance with the present invention. Typically a plurality of such devices together with external structures such as test devices and scribe channels will be fabricated as part of the total semiconductor wafer level package. For clarity, these well-known external structures are omitted from the drawing and only a portion of the semiconductor wafer level package 21, which contains device 12. The device 12 is fabricated on a semiconductor substrate wafer 11, which comprises a wafer of semiconductor material before the wafer has been diced into a plurality of distinct chips. Device 12 may be any of the devices, which are commonly fabricated using the semiconductor wafer. Typically such devices are integrated circuit structures, micromachined sensors such as accelerometers, and other micromachined structures. The device 12 may be located in one or any of three regions in the package 21. The first

location of a device 12a is inside a cavity 17 formed by the protective cap 16, the frit glass layer 14, and the substrate 11. A second location of a device 12b may be in a position beneath the frit glass 14 in which a sealing surface or the hermetic bond is formed with device 12b. Thirdly, a device 12c may be located outside the protective cap and will be exposed to external environments, electrical contacts, etc.

The cap wafer, which can be silicon, glass, metal, polymer, or the like, is provided which can be prepared by providing a plurality of holes, which extend completely through cap wafer. These holes, which are normally drilled or etched before bonding, may also be made after bonding. A frit glass is then typically deposited on the cap wafer by a silk screening method, which leads to a pattern aligned with the electrical patterns on the device wafer. Other methods of deposition may also be employed such as spin coating, spraying, direct write, etc. The preferred embodiment is to deposit slurry comprising a mixture of organic binder, solvent, and a frit glass containing filler, deposited through the silk screen. The combination is fired by heating to a high enough temperature to volatilize organic or inorganic materials. Selection and use of the binder as well as the subsequent firing comprise methods well known in the art of frit glass deposition. Then frit glass itself is selected to allow bonding below the temperature at which aluminum forms an alloy with silicon, approximately 570 degrees Celsius, and more importantly, at a low enough temperature

not affect the functionality of the electronic devices which may contain integration on the same chip, such as an IC device and sensor.

Suitable glasses may be available from VIOX Corporation, Nippon Electric Glass America, Inc., Ferro Corporation, or others, but the practiced embodiment employs a glass, identified as VIOX Glass No. 24925, or VIOX Glass No. 24927 from VIOX Corporation.

The cap wafer is bonded to semiconductor substrate wafer using a frit glass layer in direct contact with the electronic device, frit glass serving as the bonding agent. Process conditions are such that the integrated circuitry, IC, and which can include sensing elements, are compatible so as not to degrade the performance and functionality of the integrated electronic devices. Specifically the range of softening temperatures for the frit glass material is less than about 500 degrees C, preferably about 300 degrees C to about 475 degrees C. A preferred thickness of the frit glass layer is about 5 microns to about 4 mils, preferably about 5 microns to about 25 microns. Other glasses with lower bonding temperatures may be available, however, in which case it is understood that the glazing and bonding temperatures may be lowered.

Cap wafer 16 is bonded to semiconductor substrate wafer 11 using frit glass 14 as a bonding agent. This bonding comprises heating the cap wafer 16, frit glass 14, and semiconductor substrate wafer 11. In this way

semiconductor wafer level package 21 is formed as part of a capped wafer structure with device 12 hermetically sealed of predetermined dimensions formed by a combination of semiconductor substrate wafer 11, cap wafer 16, and frit glass 14. Cap wafer 16 is formed from a material, which will form a suitable seal with the frit glass. Typical such materials are semiconductor wafers, such as silicon, II-VI or III-V compound semiconductors, quartz plates, alumina plates, certain metals, polymers, or the like. The material, which comprises cap wafer 16, may be selected to provide a desired thermal expansion characteristic. For example, a silicon wafer used for cap wafer 16 will inherently have virtually identical thermal properties with a similar silicon wafer, which is used for semiconductor substrate wafer 11. The compatibility of the frit glass material of the invention provides a means to hermetically seal the device on the semiconductor substrate by directly contacting the frit glass material to the device 12 without damage or ill effects to the device. The low temperature frit glass material of the invention may also be used to form frit glass walls by predetermining the pattern of the frit glass material prior to depositing it on the surface of the cap wafer 16.

A plurality of metal traces 19 may be fabricated on semiconductor substrate wafer 11, prior to the formation of the frit glass layer 14. Metal traces 19 form a seal with the frit glass 14 as shown in Figure 1. Metal traces 19 form a plurality of electrodes on semiconductor substrate wafer 11, which provide electrical coupling to device 12. Prior to frit glass application, holes

may be etched in cap wafer 16 in locations which provide ready access to a portion of the electrodes formed by metal traces 19. A plurality of traces 19 is bonded to a plurality of pads formed on device 12 in the opening 18. Wires (not shown) extend through the opening 18 and are themselves coupled to external leads. Wires through opening 18, and metal traces 19 provide a simple, inexpensive method to provide a plurality of desired electrical couplings to device 12 while allowing portions or all of device 12 to remain hermetically sealed under the cap wafer 16.

Cap wafer 16 and semiconductor substrate wafer 11 may be aligned optically by means of opening 18, and an appropriate alignment target formed on semiconductor substrate wafer 11. Alternatively a plurality of bonding pads formed as part of metal traces 19 are used for visual alignment. The capped wafer structure is then introduced into a controlled environment, which typically comprises an inert gas at a specified pressure such as helium, argon or nitrogen. While in the inert gas, cap wafer 16 and semiconductor substrate wafer 11 are heated to bond them together to form semiconductor wafer level package 21. The bonding hermetically seals the capped wafer structure. The controlled environment is possible which provides a predetermined damping action for mechanical motion of device 12. The predetermined damping action is readily controlled by altering the composition and pressure of the inert gas. The capped wafer structure is then diced into a plurality of composite chips by sawing, a method well known in the semiconductor art. The composite chips may then be further

encapsulated, for example, within a plastic material or underfilled as is conventionally know in flip chip technology. The composite chips can also exist without further encapsulation.

While the above is an integrated device, which may contain several circuits, sensors, and other discrete integrated electrical components, alternative embodiments are possible. These can include device 12 being a device which is fabricated separately from semiconductor substrate wafer 11 then mounted on semiconductor substrate wafer 11, or other suitable substrate such as a glass plate. Other embodiments include device 12 comprising any of the devices, which are commonly fabricated using a semiconductor wafer. In these embodiments, device 12 may comprise integrated circuit structures, sensors such as accelerometers, and micromachined structures. Certain alternative embodiments deposit frit glass on a surface of semiconductor substrate wafer 11. Many embodiments combine a plurality of device structures within a cavity 17, for example an accelerometer with the associated control circuitry. Other alternative embodiments utilize alternative methods well known in the art to form frit glass bonding. These methods include defining the pattern of frit glass by photolithography. Still other methods for deposition of frit glass include: a syringe or needle, electrophoretic deposition, use of a centrifuge, direct glass paste injection through an orifice, spin coating, or spray coating.

A second preferred embodiment of the package 21 does not contain a cap wafer and is illustrated in Figure 2. The package 21 is prepared as described except the step of forming a cap wafer is omitted. The frit glass is applied directly on the device and an opening is provided in the frit glass layer to provide access to the substrate of the wafer.

EXAMPLE

A whole cap wafer or cap wafer containing cavities was selected and a glass paste pattern printed on a surface of the cap wafer by screen printing. It may be appreciated that any conventional patterning technique may be used, such as screen printing, spin coating, direct dispense writing, or photolithographic techniques. The frit glass paste was dried on the cap wafer in an oven set at 80 degrees C for 1 hour and for a second hour at 120 degrees C. The glass patterned wafers were removed from the drying oven and loaded into furnace boats. The wafers were glazed in a specified temperature program, i.e. 450 degree C temperature for at least 30 minutes. Temperature range example: min. 420 degrees C and max. 505 degrees C. The cap wafer was aligned to the device wafer in an Electronic Vision Model EV 450 Wafer Aligner in preparation for bonding of cap wafer to device wafer. In the wafer to wafer bonding step, the wafer was bonded in an Electronic Vision Model EV AB1PV Wafer Bonder Single Chamber at 430 degrees C for 10 minutes. Wafers are typically bonded 20 to 30 degrees below the glazed wafer temperature.

In the second embodiment, a whole device wafer or device wafer containing cavities or recesses was selected and a glass paste pattern printed on a surface of the wafer by screen printing. Any conventional patterning technique may be used, such as screen printing, spin coating, direct dispense writing, or photolithographic techniques. The frit glass paste was dried on the wafer in an oven set at 80 degrees C for 1 hour and for a second hour at 120 degrees C. The glass patterned wafers were removed from the drying oven and loaded into furnace boats. The wafers were glazed in a specified temperature program, i.e. 450 degree C temperature for at least 30 minutes to volatilize the organic binder. Temperature range example: about 420 degrees C and to 505 degrees C.

By now it should be clear that the present invention provides packaging devices which are fabricated on a semiconductor wafer before that wafer is diced into individual chips. The packages contain a hermetic seal by means of frit glass on electronics having thermal characteristics which closely match those of the device. The package is inexpensive to manufacture and provides for electrical connections to the device without compromising the other characteristics of the package.

We claim:

1. A semiconductor wafer level package (21) comprising:

at least one device (12) fabricated on a semiconductor substrate wafer wherein the semiconductor substrate wafer has not been diced into a plurality of distinct chips;

a cap wafer (16) having a predetermined pattern of a low temperature frit glass layer (14) deposited on a surface of the cap wafer such that a portion of the frit glass layer is in direct contact with the at least one device;

a hermetic seal formed by bonding the cap wafer (16) to the semiconductor substrate wafer using the frit glass layer (14) as a bonding agent such that the at least one device is hermetically sealed in a chamber formed by a combination of the semiconductor substrate wafer, the cap wafer and the frit glass layer;

at least one electrode formed on the surface of the semiconductor substrate wafer which provides electrical coupling to the device fabricated on the semiconductor substrate wafer; and

a hole (18) fabricated in the cap wafer which provides access to a portion of the electrode from outside the cavity.

2. The semiconductor wafer level package of claim 1 wherein the predetermined pattern of the frit glass layer (14) is deposited by a silk screening process.

3. The semiconductor wafer level package of claim 1 wherein the device (12) comprises a micromachined sensor.

4. A semiconductor wafer level package (21), comprising:

at least one device (12) fabricated on a semiconductor substrate wafer wherein the semiconductor substrate wafer has not been diced into a plurality of distinct chips;

a cap wafer (16) having a predetermined pattern of a low temperature frit glass layer (14) deposited on a surface of the cap wafer such that a portion of the frit glass layer is in direct contact with the at least one device;

a hermetic seal formed by bonding the cap wafer to the semiconductor substrate wafer using the frit glass layer as a bonding agent such that the at least one device is hermetically sealed in a chamber formed by a combination of the semiconductor substrate wafer, the cap wafer and the frit glass layer; and

a controlled environment sealed within the chamber which comprises an inert gas having a predetermined pressure which provides a predetermined mechanical damping of the device.

5. A semiconductor wafer level package (21) comprising:

at least one device (12) fabricated on a semiconductor substrate wafer wherein the semiconductor substrate wafer has not been diced into a plurality of distinct chips;

a predetermined pattern of a frit glass layer (14) deposited on a surface of the substrate wafer such that a portion of the frit glass layer is in direct contact with the at least one device (12) and an opening is defined in the pattern of the frit glass to provide access to the a portion of the substrate wafer;

a hermetic seal formed by the frit glass layer (14) deposited on the surface of the substrate wafer; and

at least one electrode formed on the surface of the semiconductor substrate wafer which provides electrical coupling to the device fabricated on the semiconductor substrate wafer.

6. The semiconductor wafer level package of claim 5 wherein the device (12) comprises a micromachined sensor.

7. A method of producing a semiconductor wafer level package (21) comprising:

fabricating at least one device (12) on a semiconductor substrate wafer wherein the semiconductor substrate wafer has not been diced into a plurality of distinct chips;

depositing a predetermined pattern of a low temperature frit glass layer (14) onto a cap wafer (16);

bonding the cap wafer (16) to the semiconductor substrate wafer using the frit glass layer (14), the frit glass layer being a bonding agent which is in direct contact with the at least one device such that the device is hermetically sealed in a chamber formed by a combination of the semiconductor substrate wafer, the cap wafer and the frit glass layer.

8. A method of producing a semiconductor wafer level package (21) comprising:

fabricating at least one device (12) on a semiconductor substrate wafer wherein the semiconductor substrate wafer has not been diced into a plurality of distinct chips;

depositing a predetermined pattern of a low temperature frit glass layer (14) onto a surface of the semiconductor substrate wafer such that a portion of the frit glass layer is in direct contact with the at least one device;

providing at least one electrode formed on the surface of the semiconductor substrate wafer which provides electrical coupling to the device fabricated on the semiconductor substrate wafer; and

fabricating an opening in the frit glass pattern to provide access to the portion of the substrate.

9. The method of claim 8 wherein the depositing step further comprises glazing the frit glass layer (14) at a temperature of less than about 500 degrees C.

10. The method of claim 8 wherein the depositing step further comprises depositing the frit glass layer (14) by a silk screening process.

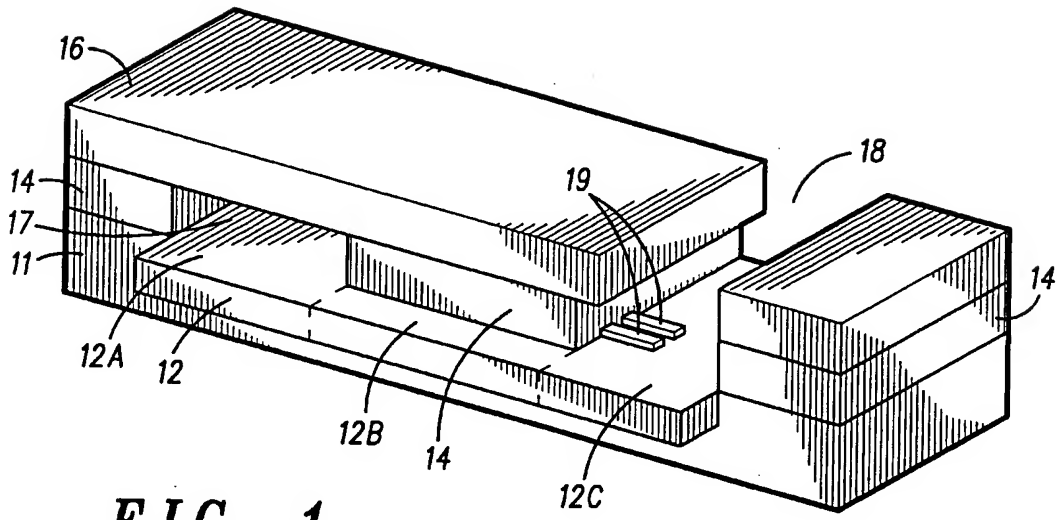


FIG. 1

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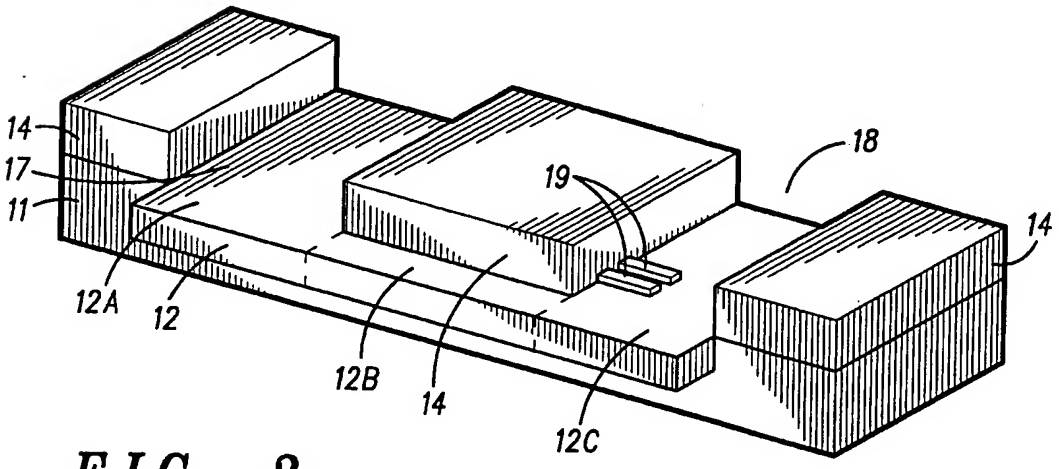


FIG. 2

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# INTERNATIONAL SEARCH REPORT

Interr nal Application No
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A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L23/04 H01L23/10 H01L21/56 H01L23/29 H01L21/52
H01L21/54

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
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C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category * | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
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☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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| Date of the actual completion of the international search | Date of mailing of the international search report |
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| 2 February 2001 | 09/02/2001 |

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